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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,032	02/06/2004	Peter Graham Laws	46309-297230	7736
23370	7590	11/30/2004	EXAMINER	
JOHN S. PRATT, ESQ KILPATRICK STOCKTON, LLP 1100 PEACHTREE STREET ATLANTA, GA 30309			RICHARDS, N DREW	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/774,032	Applicant(s) LAWS, PETER GRAHAM	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2 and 5-13 is/are rejected.
- 7) ☒ Claim(s) 3 and 4 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## **DETAILED ACTION**

### ***Priority***

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in the United Kingdom on 2/6/03. It is noted, however, that applicant has not filed a certified copy of the 0302735.6 application as required by 35 U.S.C. 119(b).

### ***Drawings***

2. Figures 1a, 1b, 2a and 2b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because the various levels of gray and black shading in the figures render the figures unclear. For instance, in figure 1, the shading used for Metal layer (n), Metal layer (n) section, and Metal layer (n-1) section appear to be almost the exact same shade such that the drawing doesn't clearly show where each of these different portions are located. Figures 2a, 2b, 3a, 3b and 5 also include this shading scheme such that it is difficult to tell which layer is which in the figures.

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Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

4. The disclosure is objected to because of the following informalities: The specification lacks a brief description of figures 1a, 1b, 2a and 2b. Page 7 lines 6-7 refer to reference numeral 19 as both an "intersection" and a "conductive island". In view of the figures it appears that reference numeral 19 is directed towards a conductive island and the first instance of reference numeral 19 in line 7 should instead recite

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reference numeral 18. The specification lacks any headings to demarcate the various sections of the disclosure. It is suggested that the specification be amended to add:

BACKGROUND OF THE INVENTION - on page 1 line 8;

SUMMARY OF THE INVENTION - on the first line of page 4;

BRIEF DESCRIPTION OF THE DRAWINGS - on page 6 line 6; and

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS - on page 6 line 20.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 5 recites the limitation "the intersect regions" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 5 depends from claim 1 which does not recite any intersect regions.

7. Insofar as definite, the claims are rejected as follows.

### ***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

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applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, 5, 6, 9 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Mori et al. (U.S. Patent No. 6,794,729 B2).

Mori et al. disclose an electrical component structure in figures 1A-18 and on columns 1-20. Specifically, Mori et al. disclose an electrical component structure in figures 2A-2C comprising:

a plurality of overlying substantially parallel layers 13/14, each layer comprising:  
a lattice comprising a first set of conductive tracks arranged substantially orthogonal to, and electrically connected with, a second set of conductive tracks; and conductive islands located in windows of the lattice, electrically isolated from the tracks thereof, wherein the lattice of one layer is electrically connected to the conductive islands of an adjacent layer (layers 13 and 14 are considered to read on the lattice and conductive islands claimed as explained below).

This is shown in figure 2A, figure 2B which is a first cross-section of figure 2A, and figure 2C which is a second cross section orthogonal to the first cross-section. Figure 2B shows the cross-section along line A-A of figure 2A and figure 2C shows the cross-section along line B-B of figure 2A.

To determine the structure of layers 13 and 14 and how they anticipate the lattice as claimed one needs to consider figures 2A, 2B and 2C simultaneously. For instance, if you consider layer 14 as shown in figure 2B, layer 14 has a window through which the via connected to electrode 10 passes and if you look at figure 2C you see that the via

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connected to electrode 10 passes through the window in layer 14 but the via connected to electrode 11 connects with layer 14. Thus, if one extrapolated the structure of layer 14 onto the top view of figure 2A, one would see that it contains a first set of conductive tracks running from left to right along figure 2A underlying electrodes 11 and a second set of conductive tracks running from top to bottom along figure 2A between electrodes 10. These two sets of conductive tracks are orthogonal to and electrically connected to each other and contain islands around the vias connected to electrode 10. The portion of the via connected to electrode 10 is considered the conductive island in the window of the layer. The same structure holds for layer 13 as well except that the lattice is offset such that the windows in layer 13 contain the vias connected to electrode 11 running therethrough. As can be seen, the lattice of one layer is electrically connected to the conductive islands of an adjacent layer. For instance, the lattice of layer 14 is connected to the conductive island (via connected to electrode 11) of an adjacent layer 13.

With regard to claim 2, intersect regions of the sets of tracks of the lattice of one layer are electrically connected to the conductive islands of an adjacent layer.

With regard to claim 5, the layers 13/14 are substantially planar as seen in figures 2B and 2C, and the electrical connection between the conductive islands of one layer and the intersect regions of an adjacent layer is established by conductive elements 12 which extend substantially perpendicular to the planes thereof. As seen in figure 2B, for example, conductive elements 12 are perpendicular to layers 13 and 14.

With regard to claim 6, the adjacent layers are separated by a material 9 having a relative dielectric constant greater than one (though the material of layer 9 is not explicitly disclosed, layer 9 is referred to as the "dielectric" layer while a further "low dielectric layer" is used around the vias, the low dielectric layer has a dielectric constant of at most 40, thus layer 9 is interpreted to have a dielectric constant of more than 40).

With regard to claim 9, Mori et al. further disclose two electrical terminals 10/11, the lattice tracks and conductive islands of each layer being respectively electrically connected to a different one of the conductive terminals.

With regard to claim 11, the structure of figures 2A-2C is a capacitor.

With regard to claim 12, Mori et al. disclose a plurality of overlying substantially planar layers 13/14, each layer comprising:

a lattice comprising a first set of conductive tracks arranged substantially orthogonal to, and electrically connected with, a second set of conductive tracks (as explained with regard to claim 1 above), crossings of the first the second sets of tracks defining intersect regions;

and conductive islands located in windows of the lattice, electrically isolated from the tracks thereof (as explained with regard to claim 1 above),

wherein adjacent layers are offset such that the conductive islands of one layer are superimposed over the intersect regions of the adjacent of the adjacent layer (the



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conductive islands of each layer are formed directly above/below the intersect regions of the adjacent layer such that they are superimposed over each other),

the lattice intersect points of the layers being electrically connected to the conductive islands of an adjacent layer by interconnecting conductive elements 12 which extend substantially perpendicular to the plane of the layers (as explained with regard to claims 1, 2 and 5 above).

With regard to claim 13, Mori et al. disclose a method of forming an electrical component comprising:

forming a plurality of overlying substantially parallel layers 13/14, each layer providing a lattice comprising a first set of conductive tracks arranged substantially orthogonal to and electrically connected with a second set of conductive tracks (as explained with regard to claim 1 above), and

conductive islands located in windows of the lattice electrically isolated from the tracks thereof (as explained with regard to claim 1 above); and

electrically connecting the lattice of one layer to the conductive islands of an adjacent layer (as explained with regard to claim 1 above).

Mori et al. is considered to have performed the steps of "forming" and "electrically connecting" as they show a structure that has the claimed layer formed and electrically connected.

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 7, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al. as applied to claims 1, 2, 5, 6, 9 and 11-13 above.

With regards to claim 7, Mori et al. teach that the vias (for instance, via 12, which constitutes the conductive island) are formed of metal (column 8 lines 10-14, for example, the via is disclosed as being a material that includes metal). However, Mori et al. does not explicitly teach the lattice tracks being formed of metal.

With regard to claim 10, Mori et al. does not explicitly teach the electrical terminal being formed by a metal plate. Mori et al. shows terminals 10 and 11 in figure 2A for example, they are shown as squares that are considered a "plate". However, Mori et al. does not explicitly teach the material they are made from.

Nonetheless, the choice of metal for the lattice tracks and electrical terminals is considered obvious to one of ordinary skill in the art at the time of the invention. In the semiconductor art, using metals as the electrodes for capacitors (i.e. the lattice tracks) and for electrical terminals is well known. Metals are commonly used because they provide a very low resistance to allow for faster signaling and processing. Thus, it would have been obvious to one of ordinary skill in the art to use metal for the lattice tracks and electrical terminals of Mori et al.

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With regard to claim 8, Mori et al. does not explicitly teach any specific material for the lattice tracks and conductive islands and thus does not teach forming them of polysilicon material. Nonetheless, the choice of polysilicon for the lattice tracks and conductive islands is considered obvious to one of ordinary skill in the art at the time of the invention. In the semiconductor art, polysilicon is known to be a common choice for electrical components. It would have been obvious to use polysilicon because polysilicon is easily formed and processed (patterned, etched, doped; allowing for easier, cheaper processing) and the use of polysilicon allows for easy integration onto a semiconductor substrate such as single crystal silicon so that the capacitor can be integrated onto the same chip as multiple other devices (higher integration increases functionality of value of IC chips). Thus, it would have been obvious to use polysilicon for the lattice tracks and conductive islands.

***Allowable Subject Matter***

12. Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to teach, disclose, or suggest, either alone or in combination, the windows of each lattice or the conductive islands having an octagonal shape. The prior art does not teach the specific shape of the conductive islands and

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windows and provides no motivation why one would choose the specific octagon shape as claimed.

### ***Conclusion***

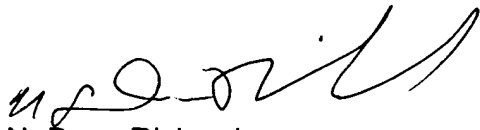
14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin et al. (U.S. Pub. No. 2003/0034546 A1), Franson et al. (U.S. Pub. No. 2003/0222328 A1), Kang et al. (U.S. Patent No. 6,600,209 B1), Appel (U.S. Patent No. 6,653,681 B2), Hu et al. (U.S. Patent No. 6,743,671 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'N. Drew Richards', is positioned above the printed name.

N. Drew Richards  
AU 2815